AMENDMENTS TO THE SPECIFICATION

IN THE SPECIFICATION:

Please replace the paragraph beginning on page 34, line 4 and ending on line 16 of the same page with the following rewritten paragraph (further to the amendment to the same paragraph as submitted in the Rule 111 Reply filed on June 19, 2003).

For the present invention it may be particularly attractive using organic materials the electrical properties of which may be modified under the influence of electromagnetic radiation, particle radiation or electric fields. Particularly it is attractive for the present invention to generate the separate main layers of one or more sublayers or such materials which is processed, either before or after the joining into one or more main layers, with the application of electromagnetic radiation with given intensities or frequency characteristics, such that the separate sublayers which are included in a main layer P, M, MP thus obtain the desired electrical properties in selected portions, for instance by the applied radiation being spatially modulated through a mask or a spatial light modulator. A process of this kind will in principle hence resemble the use of

~~photolitographic~~ <u>photolithographic</u> processing in common semiconductor technology.

Please replace the paragraph beginning on page 34, line 17 and ending on page 35, line 6 with the following rewritten paragraph (further to the amendment to the same paragraph as submitted in the Rule 111 Reply filed on June 19, 2003).

In the present invention the separate main layer, be it a processor layer P or a memory layer M, may be built up by sublayers which shall be provided with different properties before they are joined into a main layer. In a memory may for instance the memory material be provided in a central sublayer and surrounded by separate electrode layers, and there may between the separate sublayers be provided separate isolating layers, such this for instance is evident from fig. 7g. Correspondingly can for instance an active device such as transistor in fig. 12 be built up by depositing sublayers 20, 21, 22, 23 with determined properties. It is, however, thinkable that the transistor structure similar to the one in fig. 12 can be realized in one and the same organic material, as the separate sublayers are processed separately before joining by

irradiation with for instance light, such that each of sublayer patterned and unpatterned obtains the desired electrical property which shall enter into the realization of a field-effect transistor in thin-film technology. This is to say that a first sublayer could be an isolator, a second sublayer a conductor, a third sublayer a semiconductor, a fourth sublayer an isolator and finally a fifth sublayer once again an electrical conductor. For use in the present invention, whether it concerns the memory unit or the processor unit it is also desired to employ active devices, for instance the transistors mentioned, wholly realized in organic material, e.g. polymers. Similarly it is of interest to among other to generate integrated circuits wholly realized in the form of thin-film polymers. As mentioned above, among others Garnier & al. has developed and patented a MIS field-effect transistor which substantially is wholly realized in polymer technology. Generally it is of interest **to** be able to realize organic field-effect transistors in thin-film technology which simultaneously allows integration of the devices.

Please replace the paragraph beginning on page 37, line 14 and ending on page 38, line 10 with the following rewritten paragraph (further to the amendment to the same paragraph as submitted in the Rule 111 Reply filed on June 19, 2003).

However, it is particularly desirable to apply materials which makes it possible to realize the sublayers in the data processing device with a well-defined mode and degree of electrical conduction in the production process and before the joining of the sublayers according to the intended function into processor layers P or memory layers M or combinations MP thereof. Such materials shall in the following in generally be denoted as convertible materials CM, as the conversion of the electronic properties of the materials may take place reversibly or irreversibly under the influence of radiation, including both photon radiation and particle radiation, heat or electrical fields. By a spatial modulation of the radiation or the electrical fields the material may be patterned, as the desired conversion of the electronic properties will be dependent on the energy supplied or the field strength applied. This is described in more detail in the above-mentioned Norwegian patent application 980385. In contrast to the above-mentioned PANI film

it will be preferred that the materials initially are in a dielectric or electric non-conducting state. Where the material CM is not influenced by the electric fields or light, it will of course retain its dielectric properties and form an isolator, while it in influenced areas depending of the degree of conversion may appear with electrical semiconducting or conducting properties. Areas in the conducting film may hence in the fabrication process stably be provided with a determined degree and mode of electrical conductivity, such that they for the purpose appear as electrical conducting and may be used for forming electrodes and current paths in the separate sublayer, or as semiconducting and forming the active material of diodes and transistors. Used as a memory material the conversion further shall be reversible, such that the material CM forms a bistable electrical switch and makes possible electrically addressable and erasable memories of the above-mentioned kind, cf. the discussion in connection with a memory shown in fig. 7a-7h. The material CM will typically be an organic material, for instance molecules, oligomers and polymers which transfers from an initial first state to a second state under influence of light in a determined ~~frequence~~ <u>frequency</u> range. It is of course

to be understood that transition between first state and the second state shall be characterized by a change in degree and mode of the electrical conductivity.

Please replace the paragraph beginning on page 47, line 20 and ending on line 23 of the same page with the following rewritten paragraph.

A brief mention will now be given of how the data processing device ~~of the intersection~~ **according to an embodiment the invention** may be used for realizing scaleable MIMD architectures and how an IRAM concept may be used for tolerating and hiding latency and downtime which may appear in a scaleable data processing device.

Please replace the paragraph beginning on page 51, line 10 and ending on page 52, line 7 with the following rewritten paragraph.

The second alternative is forming a set of processors and memories, respectively in separate processor layers P or in separate memory layers M or in combined processor and memory layers MP. Any processor CPU shall be able to access any memory

module MM over a switching network SN, such this is shown in fig. 25. The set of memory modules MM0, MM1,... defines the global address space which is shared by all processors CPU0, CPU1,... Parallel architectures of this kind ~~is~~ **are** called MIMD computers with shared memory system and are usually denoted as multiprocessor systems, while it has been common to call MIMD architectures with distributed memory systems for multicomputers. [[-]] As also the latter can be integrated on a data processing device according to **an embodiment of** the invention, the latter denomination, however, is less precise and should perhaps best be reserved for physically separated data processing devices connected in networks. [[-]] Depending on topology the switching network in MIMD architectures may be classified as static or dynamic networks. In static networks the switching units are permanently connected and typically realized as direct lines or connections from point to point. Usually MIMD architectures with decentralised memory systems may be based on static networks, while dynamic networks substantially are used in multiprocessor computers, i.e. MIMD architectures with shared memory system. In MIMD architectures with distributed memory system the network essentially will be occupied with transmitting complete messages

which may be of any length, and message transmitting protocols
are hence of great importance in systems of this kind. In MIMD
architectures with shared memory system short, but frequent
memory access characterizes the common use of the network. MIMD
architectures with distributed memory systems offers special
problems in programming, while MIMD architectures with shared
memory usually are easy programmable, as it is not necessary to
partition the code or the data and neither is it necessary to
physically move data when two or more processors communicate.
The disadvantages of MIMD architectures with shared memory
system are the synchronization and problems with scalability due
to memory conflicts, a problem which increases with a number of
processors. A corresponding scaling of the memory capacity, i.e.
the RAM capacity has turned out to be difficult due to the
latency problems and the restrictions in the RAM capacity in
general.

Please replace the paragraph beginning on page 53, line 22 and ending on line 27 of the same page with the following rewritten paragraph.

In the data processing device according to the present invention it is supposed that this partly unsolved problem shall be less essential due to the almost unlimited scaling possibility on all functional levels. The transfer of large data volumes shall essentially comprise transfer of already processed data to external memories and ~~peripherial~~ **peripheral** devices, for instance display devices.

Please replace the paragraph beginning on page 55, line 5 and ending on page 56, line 10 with the following rewritten paragraph.

As already mentioned, an IRAM concept may be used in the data processing device according to the present invention, preferably such that a dedicated processor is assigned to each separate RAM and connected with this RAM, and the only task of which will be accessing and retrieval therein, while the CPUs of the processing unit wholly will be free for exclusively handling the execution of logic and arithmetic operations. A fundamental

realization of a combined IRAM and CPU layout is shown in fig. 26 which exploded in separate layers shows a processor/IRAM module in the data processing device according to the invention. It is to be understood that the embodiment shown therein substantially corresponds to configurations on the first and second level of the functional hierarchy. In fig. 26 the lowermost layer forms the substrate S and comprises the processor interface 3 which herein is shown as a combined control and communication processor 30. The control and communication processor 30 is via the processor bus 4 connected with an I/O circuit 31 which in its turn is connected with I/O interface 8 in order to realize communication with external devices and ~~peripherial~~ **peripheral** equipment. Single lines 33 also connect the control and communication processor 30 with the I/O circuit 31. A further circuit 32 is provided on the substrate S and similarly connected with the control and communication processor 30 over the processor bus 4. This further circuit 32 may according to need be implemented as a dedicated circuit, for instance in the form of a programmable codec. The symbol Δ on the control and communication circuit 30 indicates that the processor bus 4 is conveyed further as a

vertical bus to the first processor layer P1 provided above the

substrate S where the processor bus 4 is branching in horizontal

buses which interconnects microprocessors or CPUs 5 provided in

the layer P_1 and with the control and communication processor 30.

This ensures that the microprocessors 5 which are here shown in

a number of 4, but in no way need to be restricted to this

number, can work in parallel. Above the first processor layer P_1

there is adjacently provided a second processor layer P_2 which is

connected to the layer P_1 via the processor bus 4. In the

processor layer P_2 a number of dedicated processors 34 is

provided and adapted to access a number of RAMs 6 provided in a

memory layer M as shown in fig. 26. This takes place via

memory/processor interfaces 7 which are provided in a separate,

not more precisely denoted layer interfoliated between the

processor layer P_2 and the memory layer M. Each IRAM processor 34

is over the respective assigned interface 7 connected with a RAM

6 in the memory layer M and serves exclusively for accessing and

retrieving of data in the uniquely assigned RAM and for further

transfer of the retrieved data on the processor bus 4 to the

microprocessors 5 for processing therein. In this connection it

is to be understood that the processor bus 4 which here is

envisaged configured as a three-dimensional processor bus, may

be implemented with herein not shown switches and multiplexers.

*Please replace the paragraph beginning on page 56, line 11
and ending on page 57, line 12 with the following rewritten
paragraph.*

The processor layers P_1 and P_2 realize a processor module

and the processor layer P_2 the interfoliated layer with

interfaces 7 and the RAM layer M realizes a IRAM module in the

data processing device according to the invention. It is, of

course, to be understood that the number of IRAM processors 7

and assigned RAMs 6 as shown in the figure, necessarily need not

to be restricted respectively to 8, but may comprise a large or

lesser number of each. Further can each RAM 6 comprise a memory

port with a width of e.g. at least 1 Kb or consist of several

memory groups with their own equally wide memory ports. In

principle the memory bandwidth provided by IRAM module **will** be

the product of a number of memory ports, the port width and the

port frequency. The processor bus 4 connects in the processor

layer P_2 the IRAM processors together over horizontal buses,

while the connection between the IRAM processors 34 via the

interfaces 7 to RAM 6 may well be formed as vertical electrical conducting structures in the layers P_2, M which forms the IRAM module in the data processing device according to the invention. In the layer M is further each RAM 6 interconnected over a horizontal memory bus 37 and further via vertical memory buses 2 which leads to a not shown memory interface 1, cf. fig. 5. The memory interface 1 provides connection to further, here not shown memories which are provided in further not shown memory layers which for instance may realize a mass memory in the storage unit in the data processing device according to the invention. This memory interface 1 has in addition its own I/O interface 9 for loading data directly to the storage units, such this is shown in the mentioned fig. 5. Also, the processor bus 4 is connected with the memory interface 9 via a vertical bus, indicated by 36 in the figure. Further lozengy symbols 35 in each layer indicate how the processor bus 4 here forms a vertical structure, which extends vertically through the layer in question.